10/813,038.

COPC

Docket No.: 251076US2DIV

OBLON
SPIVAK
McCLELLAND
MAIER
&
NEUSTADT
P.C.

ATTORNEYS AT LAW

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Inventor: Yuuichi HIRANO, et al.
Patent No.: 6,975,041
Issued: December 13, 2005
Group Art Unit: 2815
Examiner: Wilson, Allan R.
For: SEMICONDUCTOR STORAGE DEVICE HAVING HIGH SOFT-ERROR IMMUNITY

Certificate
APR 0 6 2006
of Correction

SIR:

Attached hereto for filing are the following papers:

REQUEST FOR CERTIFICATE OF CORRECTION
CERTIFICATE OF CORRECTION FORM PTO 1050 (IN DUPLICATE), COPY OF AMENDMENT FILED JUNE 6, 2005, COPY OF DATE-STAMPED FILING RECEIPT

Our check in the amount of $0.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Michael E. Monaco
Registration No. 52,041

Customer Number
22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/04)
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APR - 7 2006

OBLON
SPIVAK
MCCLELLAND
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&
NEUSTADT
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Docket No.: 251076US2DIV

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RE: Inventor: Yuuichi HIRANO, et al.
Patent No.: 6,975,041
Issued: December 13, 2005
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DOCKET NO.: 251076US2DIVdec

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yuiichi HIRANO, et al.

PATENT NO.: 6,975,041 GROUP: 2815

ISSUED: December 13, 2005 EXAMINER: Allan R. Wilson

FOR: SEMICONDUCTOR STORAGE DEVICE HAVING HIGH SOFT-ERROR IMMUNITY

REQUEST FOR CERTIFICATE OF CORRECTION

DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
ALEXANDRIA, VA 22313-1450

SIR:

The following is a Request for Certificate of Correction in Serial Number 10/813,038, now U.S. Patent Number 6,975,041.

In accordance with the provisions of Rule 322 of the Rules of Practice, which implement 35 USC 254, the U.S. Patent and Trademark Office is respectfully requested to issue a Certificate of Correction in the above-identified patent. The facts are as follows:

Applicants submitted an Amendment under 37 CFR §1.114 concurrently with a Request for Continued Examination on June 6, 2005. A Notice was issued in response on June 27, 2005. The patent issued without the amendments to the claims of June 6, 2005. A copy of the Amendment as filed is attached along with a copy of the date-stamped Filing Receipt.

In light of the fact that the errors were the fault of the U.S. Patent and Trademark Office, no fees are required. The requested corrections are listed on FORM P.T.O. 1050.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 11/05)

Michael E. Monaco
Registration No. 52,041

APR - 7 2006

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 1 through Column 14, line 18, please replace the incorrect claims with the following:

Claims 1-3 (Canceled).

Claim 4. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 5. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

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CERTIFICATE OF CORRECTION

PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 6. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

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DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and PMOS transistor having its gage electrode connected to said second power supply.

Claim 7. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

Claim 8. The semiconductor storage device according to claim 7, which comprises a plurality of said first resistance-adding transistors.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 9. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gage electrode connected to said first or second impurity-containing region.

Claim 10. The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

Claim 11. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

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PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said work line.

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said work line.

Claim 12. The semiconductor storage device according to claim 4, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 13. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

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PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gage electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetween,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.

Claim 14. The semiconductor storage device according to claim 5, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 15. The semiconductor storage device according to claim 6, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

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PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 16. The semiconductor storage device according to claim 7, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 17. The semiconductor storage device according to claim 9, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 18. The semiconductor storage device according to claim 11, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 19. The semiconductor storage device according to claim 13, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

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INVENTOR(S): Yuuichi HIRANO, et al.

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Column 12, line 1 through Column 14, line 18, please replace the incorrect claims with the following:

Claims 1-3 (Canceled).

Claim 4. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 5. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

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said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 6. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

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wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and PMOS transistor having its gage electrode connected to said second power supply.

Claim 7. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

Claim 8. The semiconductor storage device according to claim 7, which comprises a plurality of said first resistance-adding transistors.

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DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 9. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gage electrode connected to said first or second impurity-containing region.

Claim 10. The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

Claim 11. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

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INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said work line.

a word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said work line.

Claim 12. The semiconductor storage device according to claim 4, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 13. A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

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INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gage electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetween,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.

Claim 14. The semiconductor storage device according to claim 5, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 15. The semiconductor storage device according to claim 6, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

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PATENT NO. : 6,975,041

DATED: December 13, 2005

INVENTOR(S): Yuuichi HIRANO, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 16. The semiconductor storage device according to claim 7, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 17. The semiconductor storage device according to claim 9, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 18. The semiconductor storage device according to claim 11, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 19. The semiconductor storage device according to claim 13, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Mailing address of sender:

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 03/02)

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By: EHK/MEMO/rca

Serial No. 10/813,038

In the matter of the Application of: Yuuichi HIRANO, et al.

For: SEMICONDUCTOR STORAGE DEVICE HAVING HIGH SOFT-ERROR IMMUNITY

Due Date: 6/4/05

The following has been received in the U.S. Patent Office on the date stamped hereon

- ■ Credit Card Form for $1,120.00
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- ■ Letter Submitting Replacement Drawing Sheets
- ■ Replacement Drawing Sheets (2)
- ■ Petition for Extension of Time 2nd month

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RCA

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:	
YUUICHI HIRANO, ET AL.	:	EXAMINER: WILSON, ALLAN R.
SERIAL NO: 10/813,038	:	GROUP ART UNIT: 2815
RCE FILED: HEREWITH	:	
FOR: SEMICONDUCTOR STORAGE DEVICE HAVING HIGH SOFT-ERROR IMMUNITY	:	

AMENDMENT

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated January 4, 2005 and the Advisory Acton dated May 13, 2005, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Amendments to the Drawings begin on page 6 of this paper and include attached replacement sheets (2).

Remarks/Arguments begin on page 7 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-3 (Canceled).

Claim 4 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 5 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 6 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising:~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor,

a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and PMOS transistor having its gage electrode connected to said second power supply.

Claim 7 (Currently Amended): ~~The semiconductor storage device according to claim 3, wherein~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode

connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

Claim 8 (Original): The semiconductor storage device according to claim 7, which comprises a plurality of said first resistance-adding transistors.

Claim 9 (Currently Amended): ~~The semiconductor storage device according to claim 3, wherein~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gage electrode connected to said first or second impurity-containing region.

Claim 10 (Original): The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

Claim 11 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a ~~work~~ word line connected to gate electrodes of said first and second access transistors,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode connected to said ~~word~~ work line.

Claim 12 (Currently Amended): The semiconductor storage device according to ~~claim 3~~claim 4, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 13 (Currently Amended): A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

~~The semiconductor storage device according to claim 3, further comprising:~~

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gage electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetween,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.

Claim 14 (New): The semiconductor storage device according to claim 5, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 15 (New): The semiconductor storage device according to claim 6, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 16 (New): The semiconductor storage device according to claim 7, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 17 (New): The semiconductor storage device according to claim 9, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 18 (New): The semiconductor storage device according to claim 11, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 19 (New): The semiconductor storage device according to claim 13, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Figures 24 and 25, labeling them as "BACKGROUND ART."

Attachments: Replacement Sheets (2)

REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 4-19 are presently active in this case, with Claim 3 cancelled, Claims 4-7, 9, 11, and 13 amended and Claims 14-19 added by the present amendment.

In the outstanding Office Action, the drawings were objected; Claim 11 was objected to; Claims 3-5 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Houston (U.S. Patent No. 4,956,815); and Claims 6-11 and 13 were indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants acknowledge with appreciation the indication of the allowable subject matter.

Claims 4-7, 9, 11 and 13 are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4-5 are further amended to recite "said first resistance-adding transistor has its gate electrode directly connected to said power supply." Claim 11 is further amended to overcome the objection noted in the Official Action. Claim 12 is amended to depend from now independent Claim 4. New Claims 14-18 correspond to Claim 12 and depend from now independent Claims 5-7, 9, and 11. New Claim 19 corresponds to original Claim 12, albeit dependent from amended Claim 13. No new matter is added.

In view of the outstanding indication of allowability and present amendment, Applicants submit Claims 6-7, 9, 11 and 13 are in condition for allowance without further comment.

Briefly recapitulating, amended Claim 4 is directed to a semiconductor storage device including a static random access memory cell. The static random access memory cell

includes a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node. The static random access memory cell also includes a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node. The first driver transistor has a first gate electrode connected to the second storage node. The second driver transistor has a second gate electrode connected to the first storage node. The semiconductor storage device further includes a first resistance-adding transistor having a first impurity-containing region connected to the first gate electrode and a second impurity-containing region connected to the second storage node. The first gate electrode is connected to the second storage node through said first resistance-adding transistor. The semiconductor storage device further includes a power supply connected to said first and second load elements, for giving a given power-supply potential. The first resistance-adding transistor is an NMOS transistor, and the first resistance-adding transistor has its gate electrode directly connected to the power supply. Applicants' claimed invention provides enhanced soft-error immunity.[1]

Houston describes a memory cell which operates in two stable states and where an asymmetry in current through the cell is required to change the state of the cell.[2] Houston further describes a circuit having nodes S1 and S2.[3] For the case where node S1 is initially logic high and node S2 is initially logic low, when attempting to write the opposite state into memory cell 2, node S1 must first be pulled to logic low. This logic low transition must be transmitted through transistor 20 which is in its most turned on state, to the common gate of transistors 6 and 8.[4] Houston specifically describes that P-channel transistors 18 and 20 inhibit nodes S2 and S1 from going to a high voltage from a low voltage state in response to pulsed transient dose radiation due to the added resistance provided in the cross-coupling by

[1] Specification, page 12, lines 5-7.
[2] Houston, abstract.
[3] Houston, Figure 2.
[4] Houston, column 3, lines 35-43.

resistive paths between source and drain regions of transistors 18 and 20 when each is in its lower conducting state.[5]

Furthermore, Fig. 2 of Houston illustrates that a gate electrode of the first resistance-adding transistor 20 is connected to a power supply VDD through transistors 18 and 22. However, Houston does not disclose a circuit where a gate electrode of a first resistance-adding transistor is directly connected to a power supply for giving a power-supply potential as recited in amended Claim 4. Similarly, Houston does not disclose a circuit where a gate electrode of a first resistance-adding transistor is directly connected to a power supply for giving a GND potential as recited in amended Claim 5.

MPEP § 2131 notes that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § 2131.02. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Because Houston does not disclose or suggest all the features recited in Claims 4-5, Houston does not anticipate the invention recited in Claims 4-5, and all claims depending therefrom.

[5] Houston, column 4, lines 8-14.

The present amendment is submitted in accordance with 37 C.F.R. § 1.116 which permits amendments placing the claims in better form for consideration on appeal after final rejection. Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Michael E. Monaco
Registration No. 52,041

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413-2220
(OSMMN 08/03)
EHK/MEMO/KKN
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